WHITE PAPER

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Fourth-Generation Field Stop IGBT with High-Performance and Enhanced Latch-Up Immunity

When tasked with developing the 4th generation 650 V rated Field Stop (FS) Trench IGBTs, Fairchild's engineers had a high bar to overcome to develop a successor to the successful 3rd generation IGBTs. To meet their design goals for achieving higher performance without sacrificing reliability or ruggedness, the design team took some novel approaches toward optimizing the sub-micron width trench and mesa cell design of Fairchild's FS technology. In doing so, they stretched the 'ideal limit of silicon' and were able to achieve a remarkable 30% reduction in switching energy loss as a result. In spite of highly increased channel density, their work resulted in very strong dynamic latch-up immunity, safely operating without failure under high-current switching of more than 3000 A/cm² under severe test conditions. The following paper was presented at PCIM Europe 2015.

IGBTs are widely used in a variety of high-power applications, such as power supplies, motor drive inverters and electric vehicles due to their low conduction and switching energy losses. Requirements for more state-of-the-art power devices for power applications have triggered development efforts industry-wide to stretch the ideal limit of silicon. These efforts focus on novel silicon-based development, as well as wide band gap material development. The theoretical silicon limit for IGBTs was investigated by Akio Nakagawa (1). In order to realize optimal silicon characteristics, various injection methods to enhance IGBT structures – such as CSTBT, IEGT and narrow mesa IGBT (2-4) – were proposed. The technology for a new generation of Fairchild FS IGBTs presented in this paper takes some of these methods into account and shows a much higher trade-off performance compared to other conventional approaches to IGBTs. Furthermore, in spite of the higher current density, the new FS IGBT showed stronger dynamic latch-up immunity under inductive load and hard current switching conditions.

In order to push IGBT silicon to the limit, extremely high electron injection efficiency from the MOS gate is required, while the hole carrier injection needs to be restricted to the level of contribution only for the conductivity modulation (1). For Fairchild's fourth-generation FS IGBTs, electron injection was enhanced with a very fine cell pitch design and a new buffer structure that restricts the hole carrier injection. The result was remarkably better trade off performance, as well as strong latch-up immunity.

Fourth-generation FS IGBTs enhance electron injection with a very fine cell pitch design

A self-aligned contact process was applied to realize the narrow mesa or high-density cathode design of the trench IGBT. This proved to be very effective in optimizing the critical dimension of active cell design for the enhanced on-state performance, as well as maximizing the latch-up current capability. In addition, multiple buffer layers were adopted for the anode side of the IGBT to effectively control the minority carrier injection during the on state and to also completely block the electric field during the off state (5). This took another step toward the silicon limit of an IGBT by showing improved trade-off performance with lower conduction and switching energy loss. Also, the enhanced switching ruggedness enables the next generation FS IGBTs to have a much higher channel density.

New Generation FS Trench IGBT

In terms of the IGBT's cathode design, the trench gate structure allows for lower conduction losses compared to a planar structure. This enables higher channel density and removes the Junction Field Effect Transistor (JFET) resistance which makes the trench structure a fascinating solution for getting the device performance closer to the theoretical limit of an IGBT as it achieves such extremely high electron injection efficiency. Additionally, for the anode side of the design, the latest IGBT technology adopts an FS layer structure to achieve further improvement because this layer increases the blocking capability and thereby reduces the necessary drift layer thickness. This reduced device thickness enables further lowering of conduction and switching energy loss, as well as a reduction in thermal resistance, which allows a smaller chip size with increased power density.

For this new generation of IGBT development, we have focused on the optimization of cathode- and anode-side engineering to achieve state-of-the-art device performance, which takes the industry another step toward achieving the ideal IGBT using silicon material. The vertical structures of the proposed IGBT are illustrated in Figure 1 for the cathode and anode sides.

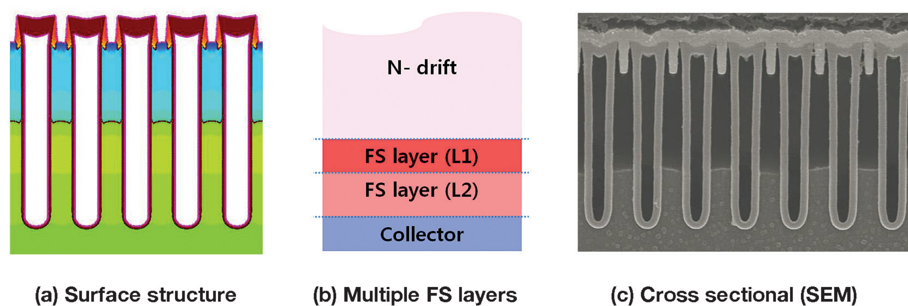


Figure 1 Proposed structure

High Density Cell Structure

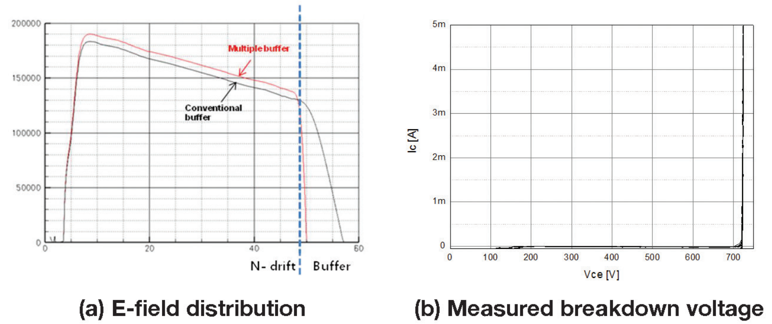
To realize the extremely high electron injection efficiency from the cathode side of the IGBT, we adopted the submicron width trench and mesa width design, with a cell pitch that is half that of our previous generation IGBT design. This fine cell pitch design could be sensitive to a process variation, such as photo misalignment, and could result in significantly varying electrical characteristics. Also, in many high power field applications, IGBTs are used in parallel for high current operation. However, if the IGBTs in a parallel application have significantly different threshold voltages or on-state voltages from each other, a very large current will flow to the IGBT that has relatively lower conduction value. So each IGBT should have as small a deviation as possible to ensure safe parallel operation. Even a single IGBT device can be affected by process variation. Many active cells comprise the single IGBT chip, so if each unit cell doesn't have a uniform doping profile, the current cannot flow evenly inside the IGBT and will crowd to the several weak local unit cells and thereby compromise the IGBT's ruggedness.

In order to overcome the process variation dependency of the device's electrical features, we employed a self-aligned contact process along with several photo processes that address the issues of active structure patterning and eliminate the factors that cause photo misalignment. The vertical structure of an IGBT fabricated with the self-aligned contact process in this experiment is illustrated in Figure 1(c). By employing the self-aligned contact process, the high-density cell design with sub-micron narrow mesa width could be implemented. The fabricated IGBTs in this experiment showed narrow electrical characteristics distribution, such

as on-state voltage and maximum saturation current level. The higher density active pattern shown in this figure is beneficial for extremely enhanced electron injection from the cathode side and, as a result, lowers the conduction loss.

Novel Multiple Buffer Layer Structure

A new, multiple buffer structure was proposed in 2013 (5) to achieve higher device performance and robust short circuit capability without oscillation of the FS trench IGBT. Generally, a conventional FS IGBT uses a single uniform buffer layer with 1~5e15cm–3 doping concentration for both hole injection control and electric field blocking efficiently. In this multiple FS layer experiment, a thin buffer layer with a much higher doping concentration was also embedded for better trade-off performance. In other words, the higher doping concentration in the double buffer layer is even more effective for electric field blocking and hole carrier injection control by the first FS layer (L1). The lower doping concentration for the second buffer layer (L2) is preferred for forming a lightly doped p-type collector for high-speed switching performance without impacting the lifetime of the device. In addition, the device's switching waveform can be effectively improved by varying the doping concentration and thickness of the double buffer layers, which ensures proper carrier distribution control during the ON/OFF switching operation.



(a) E-field distribution **(b) Measured breakdown voltage**

Figure 2 Static avalanche breakdown mode

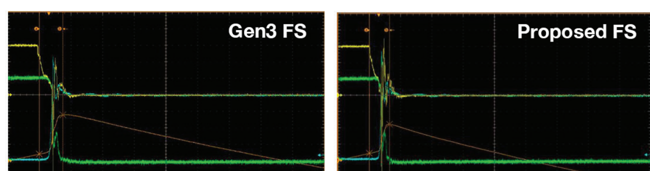
Experiment and results

Static characteristics

Because lifetime control was not used for the FS IGBT development in this work, the on-state voltage drop depends mainly on the current gain through the anode engineering with multiple FS layers. Therefore, optimization of the anode condition is critical for the overall trade-off in performance, and the switching performance is also directly influenced by the current gain of the device. The on-state voltage drop of the proposed FS trench IGBT was 1.65V at 470A/cm^2 while showing a positive temperature coefficient over a current density of 90A/cm^2, which is useful for parallel operations. Having multiple buffer layers that are highly optimized is also important for the proper electrical field blocking under static avalanche breakdown mode. The simulated electric field distributions comparing conventional FS layers are illustrated in Figure 2(a) and the measured breakdown voltage is about 720V with a very hard waveform as shown in Figure 2(b). This shows that the multiple buffer layers are sufficiently blocking the electric field in the off state.

Turn-off switching characteristics

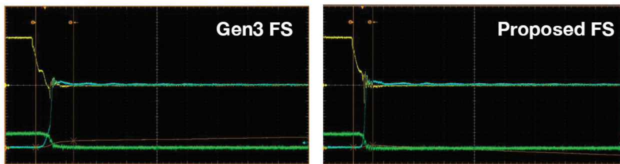
High-speed turn-off switching was also achieved with multiple buffer layers and gate capacitance optimization without any lifetime control. The switching characteristics of the proposed FS4 trench IGBT was measured under a inductive load switching test circuit in Figure 3(a). The test conditions were Vcc=400V, Vge=15V, Jc=470A/cm^2 with 6 ohm gate resistance. Compared to previous generation IGBTs, the FS4 trench IGBT showed a 30-percent lower turn-off energy loss



(a) Turn-off switching at rated current (Jc 475A/cm^2)

Figure 3 Turn-off switching waveforms

at the same on-state voltage drop. Additionally, the turn-off switching at lower current conditions is very important because the operating current level in the actual application is generally lower than the rated current. To achieve the necessary high-speed switching even under lower current conditions, carrier distribution control was used to control Vce slope during the turn off transient. The Vce waveform during low current switching has two slopes and the first slope has been improved by carrier distribution optimization with anode and cathode engineering, which is the status before an electric field touches the buffer layer. The measured switching waveforms under low current switching with $Jc=95A/cm^2$ are compared in Figure 3(b) for the proposed device and the conventional device.



(b) Turn-off switching at low current (Jc 95A/cm²)

Figure 3 Turn-off switching waveforms

Trade-off performance

Trade-off performance has been compared between the third generation and fourth generation FS trench IGBT in terms of conduction and switching energy loss in Figure 4. The fourth generation FS IGBT shows better trade-off performance compared with previous generation IGBT technology – about 30-percent turn-off energy loss (Eoff) reduction at the same on-state voltage. Compared to the previous generation IGBT,

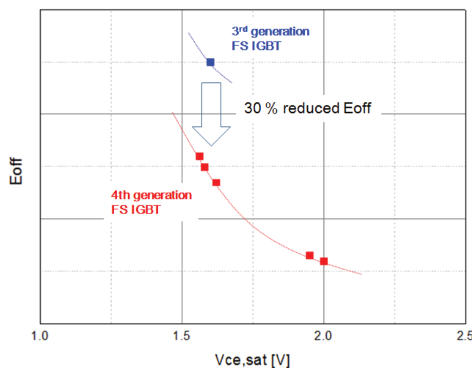


Figure 4 Trade-off performance

increased channel density with reduced gate capacitance and restricted minority carrier injection from anode side was effective for the improved trade-off performance.

Latch up immunity

For the planned fourth-generation IGBT, the channel density has been increased while the chip size has been reduced, which dramatically increases the power density. This has traditionally been a concern because increased power density increases the possibility of latch-up. The FS4 trench IGBT technology showed strong latch-up ruggedness in spite of the high-power density and with a smaller active size than previous generation IGBT technology. The latch-up immunity was evaluated under static and dynamic conditions, as shown in Figures 5 and 6 respectively. Figure 5 shows that the maximum static saturation current is around $4000A/cm^2$ with no latch-up occurring. In particular, for the dynamic latch-up characteristics shown in Figure 6, the proposed FS IGBT shows a very strong ruggedness and also safely operates over a $3000A/cm^2$ current density without failure while under the severe hard switching conditions (T=150°C, Rg=0Ω, Vge=±15V to induce very high voltage slop (dv/dt) between collector and emitter). This is because the self-aligned process removes any possible local weak points from the contact photo misalignment so that the injected minority

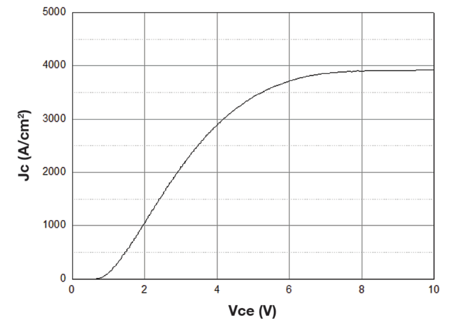


Figure 5 Static latch-up characteristics

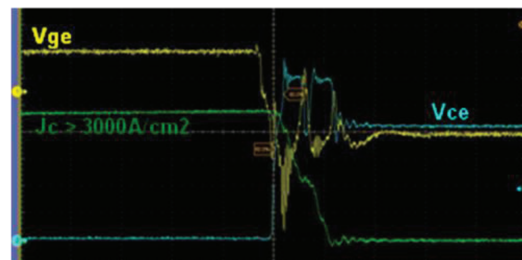


Figure 6 Dynamic latch-up characteristics

carrier can evenly flow without crowding into any specific area.

Conclusion

In summary, the fourth-generation FS IGBT technology was successfully developed using the injection enhanced carrier profile that was optimized in an effort to approach the limits of IGBT silicon. This new generation of FS IGBTs with a high-density cell structure and well-designed double buffer layer shows superior device performance under static and dynamic states as well as strong latch-up ruggedness. We've confirmed that the self-aligned process is a very effective method for the embodiment of sub-micron trench and mesa active design, as well as for realizing strong latch-up immunity. For following iterations of IGBT development, the mesa width will be narrowed further using the self-aligned process. This will further maximize the injection enhancement and accordingly the buffer structure for the minority carrier injection control should be optimized.

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